**EET380-Digital communications I**

**Unit 4 Lab**

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**ABSTRACT**

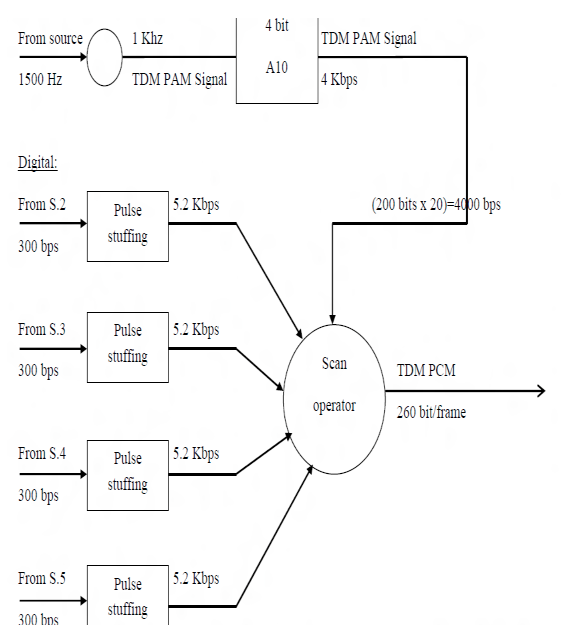
The mission of this project is to implement a 5-channel TDM-PCM transmitter and receiver.

**INTRODUCTION**

Presented in this Lab is an experiment that is to be conducted using multisim software. At the end of the lesson, one should be comfortable to successfully explain the observations and state the results.

**Methods and procedures**

The structure is with one analog signal and four digital signals. The 500 Hz analog signal is converted into a PAM signal at 1 KHz; with 4-bits encoding, this becomes a 4 Kbps PCM digital bit stream. A simple multiplexing technique is to use a 260 bit frame, with 200 bits for the analog signal and 15 bits for each digital signal, transmitted at a rate of 5.2 Kbps or 20 frames per second. Thus the PCM source transmits an (20 frames/sec) x (15 bits/frame)=300 bps.



The resolution *Q* of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete values:

Q = EFSR/2M

where *M* is the ADC's resolution in bits and *E*FSR is the full scale voltage range (also called 'span'). *E*FSR is given by

EFRS = VRefHi - VRefLow

where *V*RefHi and *V*RefLow are the upper and lower extremes, respectively, of the voltages that can be coded.

Normally, the number of voltage intervals is given by

N = 2M a 3-bit ADC divides the range into 23 or eight divisions. A binary or digital code between 000 and 111 represents each division. The ADC translates each measurement of the analog signal to one of the digital divisions. Figure 10 shows a 5 kHz sine wave digital image obtained by a 3-bit ADC. As shown in figure 11, the digital signal does not represent the original signal adequately because the converter has too few digital divisions to represent the varying voltages of the analog signal. However, increasing the resolution to 16 bits to increase the ADC number of divisions from eight (23) to 65,536 (216) allows the 16-bit ADC to obtain an extremely accurate representation of the analog signal. This inherent uncertainty in digitizing an analog value is referred to as the Quantization error. The quantization error depends on the number of bits in the converter, along with its errors, noise, and non-linearities.

Thus, given a resolution (such as 16 bits), the number of binary levels may be calculated using:

No of levels = 2 resolutions= 216 = 65,536 Levels

Further, given a Device Input Range (such as 0V to 10V) of a given signal, the code width may be calculated using:

Code width = Device input Range/ 2Resolution =10V/216 = 305 microvolts

Compare 16-bit resolution to 3-bit resolution (8 levels and 1.25V code width) in the following figure.

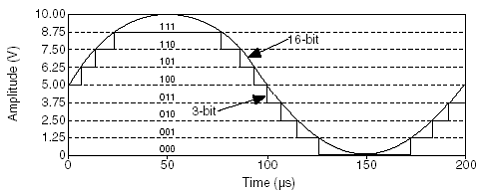
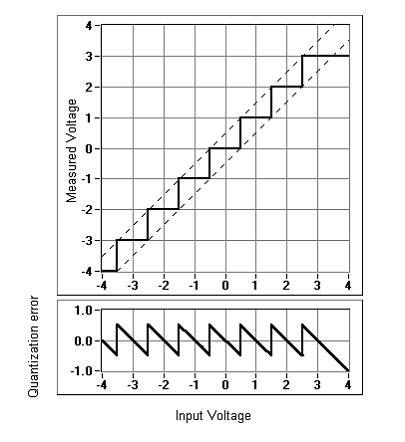
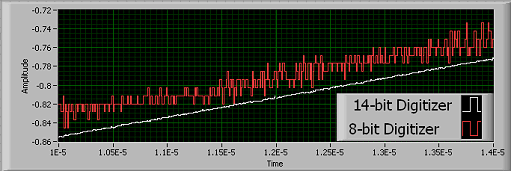
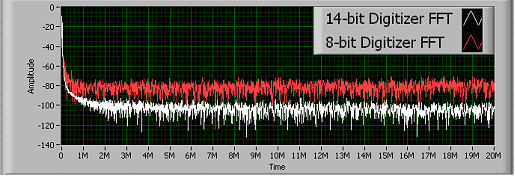
  **Figure 10. Digital image of a 5 kHz sine wave obtained by a 3 bit ADC**   **Figure 11. Quantization error when using a 3 bit ADC**

Figure 12 shows what it would look like to acquire a signal given a 2.5 V input range using a 14-bit digitizer (NI 5122 High-Speed Digitizer) vs. an 8-bit digitizer (NI 5112 High-Speed Digitizer). You can see the accuracy gained with the 14-bit digitizer given the fact that it has 16,384 discrete voltage steps to represent the input signal compared to 256 levels for an 8-bit digitizer or oscilloscope.

**Conclusion**

Using high-resolution digitizers also give you the ability to take multiple types of time AND frequency domain measurements using one instrument. This graph clearly shows the advantages of using a high resolution digitizer for time domain and frequency domain measurements.  • 8-bit = 256 discrete levels • 12-bit = 4,096 discrete levels • 14-bit = 16,384 discrete levels





**Reference:**

Digital fundamentals- Thomas Floyd